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| 10/777,739 | 02/11/2004 | Robert E. Ober | J0658.0009 | 5608 |

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| EXAMINER | |
|---|---|
| THAI, TUAN V | |

| ART UNIT | PAPER NUMBER |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/777,739 | OBER ET AL. | |
| | Examiner | Art Unit | |
| | Tuan V. Thai | 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3 and 6-11* is/are pending in the application.

4a) Of the above claim(s) *4,5 and 12-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6 and 8-11* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

**Part III DETAILED ACTION**

***Response to Amendment***

1. This office action is in response to Applicant's communication filed February 26, 2008. Claims 1-3 and 6-11 are presented for examination. Claims 4-5 and 12-34 have been canceled.

2. Applicant's arguments with respect to claims 1-3 and 6-11 have been fully considered but they are not deemed to be persuasive.

***Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 and 10-11 are rejected under 35 U.S.C. 103(a as being unpatentable over Janik et al. (USPN: 6,754,116); hereinafter Janik, in view of Simpson (USPN: 5,287,470).

As per claim 1, Janik discloses a memory system comprislng a multi-bank memory having a first memory bank and a second memory bank (e.g. see figure 2); a muxing circuit coupled to the multi-bank memory (e.g. see figure 2); a first memory access device coupled to muxing circuit is taught as processor 3 (e.g. see figure 2); and a second memory access device coupled to the muxing circuit is taught as BITST 2 (e.g. see figure 2); wherein the muxing circuit is configurable to couple the first access device to the first memory bank and the second memory bank to read and write on-interleaved data, and the muxing circuit is configurable to couple the second access device to the first memory bank and the second memory bank to read and write non-interleaved data (e.g. see figure 2; column 2, lines 48 et seq.; column 3, lines 16 et seq.; column 5, lines 41-48). Janik discloses the invention as claimed. Janik, with on exception, does not particularly disclose the simultaneous access operation amongst the memory banks. Simpson, in his teaching of processing system for coupling multi-lead output bus to interleaved memories includes

coupling circuitry operable to couple bus leads to input nodes of two subset bank of memories, discloses simultaneous-access-operation is allowed to any two different interleaved-memory-banks to increase data accessing rate (e.g. see column i0, lines 31-34). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to utilize the teaching of Simpson for that of Janik in order to allow for simultaneous accessing of interleaved-memory-banks that is currently amended in claim 1 of the invention. In doing so, Simpson clearly teaches that data bandwidth is significantly increased, results to enhancing of data throughput; therefore being advantageous (e.g. see column 3, lines 34-41; also see column 10, lines 31-34).

As per claim 2, the third memory is embedded in the system of Janik as multiple banks being taught wherein the muxing circuit is configurable to couple the first access device to the third memory bank and the muxing circuit is configurable to couple the second access device to the third memory bank (e.g. see column 5, lines 41 et seq.).

As per claim 3, Janik discloses a third memory (coupling to external line 5, figure 2) access device

coupled to the muxing circuit and wherein the muxing circuit is configurable to couple the third access device to the first memory bank and the second memory bank (e.g. see column 8, lines 9 et seq.).

As per claim 10, Janik discloses the first memory access device is processor 3 (e.g. see figure 2).

As per claim 11, Janik further discloses the second memory access device is a DMA controller or BIST 2 (e.g. see figure 2).

5. Claims 6 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Janik et al. (USPN: 6,754,116); hereinafter Janik, in view of Simpson (USPN: 5,287,470) and further in view of Carnevale (USPN: 6,430,648).

As per claims 6 and 8-9, Janik and Simpson disclose the size of memory banks is a system dependent feature (e.g. see Janik's column 2, lines 3 et seq.; column 8, lines 61 et seq.). Janik and Simpson do not particularly disclose the first memory bank is larger than the second memory bank, and wherein the first memory bank is of the first memory type being DRAM, and the second memory bank is of the second memory type being SRAM. Carnevale, in his teaching of arranging address space to access multiple

memory banks, discloses the missing elements that are known to be required in the system of Janik and Simpson in order to arrive at Applicant's current invention wherein Carnevale discloses his system comprises multiple memory banks of different types and sizes, wherein the first type being DRAM and the second memory type being SRAM (e.g. see column 1, lines 62 et seq.; column 4, lines 45 et seq.). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to utilize the teaching Carnevale and to implement the first memory bank is larger than the second memory bank (since the bank size can be of different sizes), and the first memory bank is of the first memory type being DRAM, and the second memory bank is of the second memory type being SRAM for that of Janik and Simpson's system. In doing so, it would increase and enhance Janik and Simpson system adaptability and allowing Janik and Simpson's system serving broader ranges of application, therefore being advantageous.

**Allowable subject matter**

6. Claim 7 is objected to as being dependent upon a rejected based claim, but would be allowable if rewritten

in independent form including all of the limitations of the base claim and any intervening claims.

7. With respect to the remark, Applicant's counsel argued that Janik and Simpson does not disclose the invention recited in sole independent claim 1 for at least two reasons. First, claim 1 recites that the muxing circuit is configurable so that the first memory access device is coupled to the first memory bank and the second memory access device is discretely and simultaneously coupled to the second memory device...; Second, claim 1 recites that the data transmitted to the memory devices is non-interleaved, but both Janik and Simpson disclose the transmission of interleaved data. (e.g. see page 8 of the remark).

Again, Examiner would like to emphasize that Janik clearly disclose the two discrete couplings as being contended by Applicant's counsel wherein Janik teaches the MUX in figure 2 coupling both the BIST processor 2 which generates single command I and the processor 3 which generates multiple command II to both memory BANK A and memory B wherein each processor can separately address each memory bank separately or simultaneously (e.g. see figure

2; also see column 3, lines 66 et seq.; column 8, lines 1 et seq.). In addition, the reference of Simpson is relied upon by the Examiner is merely for concept of simultaneous access operation amongst the memory banks wherein Simpson clearly discloses simultaneous-access-operation is allowed to any two different interleaved-memory-banks to increase data accessing rate (e.g. see column I0, lines 31-34; also column 10, lines 31-34); Janik reference discloses the MUX circuit configured to create two discrete couplings as stated above; the rejection of the claims based on the combination of Janik and Simpson in order to arrive at Applicant claimed invention is therefore proper. The transmission of non-interleaved data to the memory is taught by Janik to the extent that it is being claimed; for example, Janik clearly discloses that each memory access device (BIST processor 2, or processor 3) can generate commands (either single or multiple bank commands) to both memory BANK A or memory BANK B) wherein Janik clearly defines each command is for reading and writing information, namely READ (RD) and WRITE (WR) (e.g. see column 8, lines 21 et seq.); it further noted that NOT all the data transmitted to the memory is interleaved data; for example, Janik discloses if a multibank command is

transmitted to the semiconductor memory, each selected memory bank is allocated the single-bank command that is intended for it and is provided by the multibank command for such memory bank, and at a fixed point in time, each memory bank is generally allocated another command. Accordingly, in a sequence of multibank commands, the sequence of those single-bank commands that an individual memory bank executes is generally different from memory bank to memory bank. The memory banks can execute an entirely different order of single-bank commands in one and the same time period (e.g. see column 4, lines 30 et seq.).

***Conclusion***

**8. THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. . 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. . 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan

V. Thai whose telephone number is (571)-272-4187. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see ***http://pair-direct.uspto.gov***. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

***TVT***/May 21, 2008

/Tuan V. Thai/
Primary Examiner, Art Unit 2186